In the Claims:

1. (Currently amended) An integrated circuit device, comprising:

a delay-locked loop (DLL) **[[**that is**]]** configured to support transition from a partial feedback loop lock condition to a full feedback loop lock condition during a start-up time interval.

2. (Currently amended) The device of Claim 1, wherein said DLL comprises:

a variable delay line **[[**that is**]]** responsive to a reference clock signal;

an auxiliary phase detector **[[**that is**]]** electrically coupled to said variable delay line; and

a main phase detector **[[**that is**]]** responsive to the reference clock signal and a feedback clock signal.

3. (Original) The device of Claim 2, wherein said auxiliary phase detector is an edge-triggered SR-type phase detector.

4. (Original) The device of Claim 2, wherein said auxiliary phase detector is an edge-triggered SR-type phase detector; and wherein said main phase detector is a three-state phase frequency detector.

5. (Original) The device of Claim 2, wherein said DLL is responsive to the reference clock signal; and wherein the transition from the partial feedback loop lock condition to the full feedback loop lock condition is synchronized with the reference clock signal.

6. (Currently amended) An integrated circuit device, comprising:

a delay-locked loop (DLL) **[[**that is**]]** configured to support a jump from a partial clock cycle lock condition in a partial feedback loop to a two or more clock cycle lock condition in a full feedback loop that comprises the partial feedback loop, during a start-up time interval.

7. (Currently amended) The device of Claim 6, wherein said DLL comprises a variable delay line **[[**that is**]]** responsive to a reference clock signal; and wherein the jump in lock condition is synchronized with the reference clock signal.

8. (Original) The device of Claim 6, wherein said DLL comprises a variable delay line and a fixed delay line that collectively define the full feedback loop.

9. (Currently amended) The device of Claim 6, wherein said DLL comprises:

a variable delay line **[[**that is**]** responsive to a reference clock signal;

an auxiliary phase detector **[[**that is**]** electrically coupled to said variable delay line; and

a main phase detector **[[**that is**]** responsive to the reference clock signal and a feedback clock signal.

10. (Original) The device of Claim 9, wherein said auxiliary phase detector is an edge-triggered SR-type phase detector.

11. (Original) The device of Claim 9, wherein said auxiliary phase detector is an edge-triggered SR-type phase detector; and wherein said main phase detector is a three-state phase frequency detector.

12. (Currently amended) The device of Claim 7, wherein said DLL comprises:

a variable delay line **[[**that is**]]** responsive to the reference clock signal;

a fixed delay line **[[**that is**]]** electrically coupled to an output of said variable delay line;

an auxiliary phase detector **[[**that is**]]** electrically coupled to said variable delay line;

a main phase detector **[[**that is**]]** responsive to the reference clock signal and a feedback clock signal **[[**that is**]** generated at an output of said fixed delay line; and

a control circuit **[[**that is**]]** responsive to the reference clock signal and a power-on reset signal, said control circuit **[[**and is**]]** configured to selectively enable said auxiliary phase detector and said main phase detector in sequence during a start-up time interval that commences upon receipt of a trailing edge of the power-on reset signal.

13. (Currently amended) The device of Claim 12, wherein said control circuit is further configured to time an enablement of the main phase detector during the start-up time interval to a count of a number of cycles of the reference clock signal.

14. (Currently amended) The device of Claim 13, wherein said DLL further comprises a multiplexer **[[**that is**]]** responsive to a select signal generated by said control circuit and having **[[**has**]]** first and second pairs of inputs **[[**that are**]]** electrically coupled to said auxiliary phase detector and said main phase detector, respectively.

15. (Currently amended) The device of Claim 12, wherein said DLL further comprises a multiplexer **[[**that is**]]** responsive to a select signal generated by said control circuit and having **[[**has**]]** first and second pairs of inputs **[[**that are**]]** electrically coupled to said auxiliary phase detector and said main phase detector, respectively.

16. (Currently amended) The device of Claim 15, wherein said DLL further comprises:

a charge pump **[[**that is**]]** responsive to UP and DOWN signals provided by said multiplexer; and

a filter having an input **[[**that is**]]** electrically coupled to an output of said charge pump and an output **[[**that is**]]** electrically coupled to bias terminals of said variable delay line.

17. (Currently amended) An integrated circuit device, comprising:

a delay-locked loop (DLL) **[[**that is**]]** configured to support a jump from half or full clock cycle locking of an auxiliary portion of a feedback loop to a two clock cycle locking of a full portion of the feedback loop during a start-up time interval.

18. (Original) The device of Claim 17, wherein said DLL is responsive to a reference clock signal; and wherein a timing of the jump is synchronized with the reference clock signal.

19. (Currently amended) The device of Claim 18, wherein said DLL comprises:

a variable delay line **[[**that is**]]** responsive to the reference clock signal;

an auxiliary phase detector **[[**that is**]]** electrically coupled to said variable delay line; and

a main phase detector **[[**that is**]]** responsive to the reference clock signal and a feedback clock signal.

20. (Original) The device of Claim 19, wherein said auxiliary phase detector is an edge-triggered SR-type phase detector; and wherein said main phase detector is a three-state phase frequency detector.